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Improving Performance via Blocking Layers in Dye-Sensitized Solar Cells Based on Nanowire Photoanodes

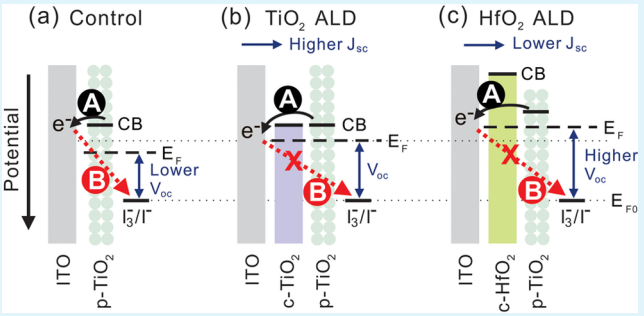
Luping Li,*[,†] Cheng Xu,[‡] Yang Zhao,[†] Shikai Chen,[†] and Kirk J. Ziegler*[,†,‡]

[†]Department of Chemical Engineering, University of Florida, Gainesville, Florida 32611, United States

[‡]Department of Materials Science & Engineering, University of Florida, Gainesville, Florida 32611, United States

Supporting Information

ABSTRACT: Electron recombination in dye-sensitized solar cells (DSSCs) results in significant electron loss and performance degradation. However, the reduction of electron recombination via blocking layers in nanowire-based DSSCs has rarely been investigated. In this study, HfO_2 or TiO_2 blocking layers are deposited on nanowire surfaces via atomic layer deposition (ALD) to reduce electron recombination in nanowire-based DSSCs. The control cell consisting of ITO nanowires coated with a porous shell of TiO_2 by $TiCl_4$ treatment yields an efficiency of 2.82%. The efficiency increases dramatically to 5.38% upon the insertion of a 1.3 nm TiO_2 compact layer between the nanowire surface and porous TiO_2 shell. This efficiency enhancement implies that porous sol–gel coatings on nanowires (e.g., via $TiCl_4$ treatment) result in significant electron recombination in nanowire-based DSSCs, while compact coatings formed by ALD are more advantageous because of their ability to act as a blocking layer. By comparing nanowire-based DSSCs with their nanoparticle-based counterparts, we find that the nanowire-based DSSCs suffer more severe electron recombination from ITO due to the much higher surface area exposed to the electrolyte. While the insertion of a high band gap compact layer of HfO_2 between the interface of the conductive nanowire and TiO_2 shell improves performance, a comparison of the cell performance between TiO_2 and HfO_2 compact layers indicates that charge collection is suppressed by the difference in energy states. Consequently, the use of high band gap materials at the interface of conductive nanowires and TiO_2 is not recommended.



KEYWORDS: *dye-sensitized solar cell, electron recombination, ITO nanowire, blocking layer, core–shell, atomic layer deposition, band gap*

1. INTRODUCTION

Dye-sensitized solar cells (DSSCs) are promising alternatives to conventional Si-based solar cells due to their low cost and ease of fabrication. After decades of research and development, efficiencies up to 13% have been reached recently.[1] The photoanode of a DSSC typically consists of a mesoporous thin film of TiO_2 attached to a transparent conductive oxide (TCO). A monolayer of a photosensitive dye, such as N719,[2] is attached to the TiO_2. During DSSC operation, electrons in the dye are excited by photons from the lowest unoccupied molecular orbital (LUMO) to highest occupied molecular orbital (HOMO) levels, which are subsequently injected into the conduction band (CB) of TiO_2. The electrons are collected by the TCO and passed through the external circuit to reach the Pt counter electrode. The I^-/I_3^- redox couple then regenerates the dye to complete the process.

Improving DSSC performance relies on maximizing photon absorption and minimizing electron recombination.[3] Conventional TiO_2 nanoparticle-based photoanodes have relatively high surface area that enables high dye loading and charge injection.[4] However, the charge transport in TiO_2 nanoparticles occurs via a random walk in a trap-limited diffusion process through the many defects and impurities in the nanoparticle film. It is estimated that under full sunlight, an electron may experience an average of a million trapping events before they reach the current collector.[4] These trapping events greatly reduce charge transport and increase the probability of electron recombination to the oxidized dye or to I_3^- in the electrolyte.[5] These processes limit the diffusion of electrons to ~10 μm.[6] Consequently, electrons generated greater than 10 μm away from the current collector will not contribute to the photocurrent because these electrons are unlikely to be collected.[7]

Nanowire-based photoanodes are promising architectures that could overcome these limitations. These devices typically consist of single- rather than poly-crystalline networks. This architecture improves electron transport because there are fewer potential barriers at grain boundaries,[8,9] providing efficient axial transport of collected electrons. Because nanowires are typically grown directly on the current collector,[4,10] a

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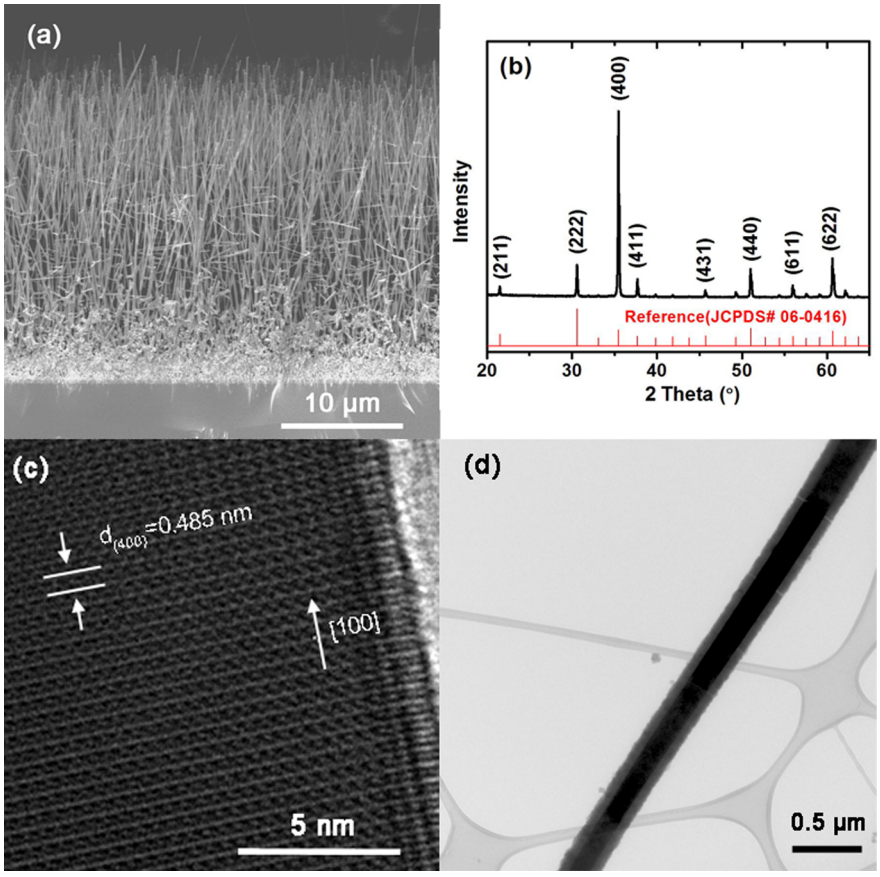

Figure 1. (a) Typical SEM image and (b) XRD pattern of as-grown ITO nanowires. (c) HRTEM image demonstrating the highly crystalline nature of the ITO nanowires. (d) TEM image of ITO nanowires coated by TiO_2 via $TiCl_4$ treatment.

continuous path to the external circuit is established. To maximize charge transport, the nanowires should be highly conductive. Electron transport through single-crystalline nanowires, such as tin-doped indium oxide (ITO) nanowires, has been shown to be an order of magnitude faster than through TiO_2 nanoparticles.[10] Coating these one-dimensional nanostructures with a thin coating of TiO_2 also limits the diffusion length of the electron to the thickness of the shell.[11] This orthogonality decouples the electron diffusion length from the photoanode thickness and may allow thicker photoanodes to be used more effectively, providing higher photocurrent. The core−shell structures also generate a radial electrical field because of band bending that facilitates electron transport and minimizes electron losses.[4,7,8,12,13] Therefore, any electrons injected into the semiconductor shell are rapidly drawn to the conductive nanowire core rather than randomly walking to the current collector. The short dwelling time for electrons in the TiO_2 shell also substantially reduces the chances of recombination. For example, it has been shown that transport dynamics can be 2 orders of magnitude faster than nanoparticle-based DSSCs.[12]

Law et al. demonstrated the first nanowire-based DSSC using ZnO nanowire arrays and obtained an efficiency of 1.5%.[4] To enhance the electric field effects, the authors later showed that a thicker TiO_2 shell (10−25 nm) on ZnO nanowires improved efficiency to 2.5%.[11] While the established electric field helped, the surface area available to the dye remained prohibitively low. To improve the surface area, Xu et al. synthesized multilayer ZnO nanowires and obtained an efficiency of 7%.[14] Further improvements to the surface area of nanowire arrays could lead to efficiencies beyond those observed for nanoparticle-based DSSCs. While physics suggests that electron recombination should be reduced in a DSSC consisting of core−shell nanowires, the higher surface area of the nanowire array may lead to detrimental effects. For example, the increase to the surface area of the current collector could make electron recombination from ITO to the electrolyte more severe in nanowire-based devices. Insertion of a compact blocking layer at the photoanode interface is an effective approach to reduce electron recombination in nanoparticle-based DSSCs.[2,5,15,16] Han et al.[17] recently reported ITO nanowires consecutively coated with a compact TiO_2 shell of 30 nm and then a porous TiO_2 shell of 70 nm, leading to a substantial improvement in efficiency to 6.1%. However, the dimensions of these compact layers are too thick for adequate tunneling and cannot be considered as blocking layers.[5,15,18] Despite the importance, reducing electron recombination in nanowire-based DSSCs through blocking layers has been rarely reported.

In this study, blocking layers are used to reduce electron recombination in ITO nanowire-based DSSCs. Vertically aligned ITO nanowires were synthesized directly on an ITO substrate, and a compact blocking layer of either HfO_2 or TiO_2 was deposited on the surface of the nanowire by atomic layer deposition (ALD). Subsequently, the nanowire surface was coated with a porous TiO_2 shell via $TiCl_4$ treatment to allow significant dye adsorption. The effect of the compact blocking layer and porous shell layer on the photovoltaic properties of the nanowire-based DSSCs is investigated. A maximum efficiency of 5.38% was achieved upon inserting blocking layers, corresponding to a 90% enhancement in efficiency.

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2. EXPERIMENTAL SECTION

2.1. Synthesizing ITO Nanowires. ITO nanowires were synthesized via a thermal evaporation method as described in our previous work.[19] Briefly, high-purity In and Sn powders were mixed at an atomic ratio of 10:4.5 and loaded into a quartz tube. Nanowires were grown on clean ITO/glass substrates (Thin Film Devices, Inc., Anaheim, CA) sputtered with a 3 nm Au film (as catalyst) in a stream of 0.5% O_2 in Ar flowing at 40 sccm. The tube furnace was heated rapidly to 750 °C and a growth time of 33 min usually led to nanowire lengths of approximately 20 μm. Scanning electron microscopy (SEM) was used to check the length of nanowires prior to device fabrication. All nanowires used in this study have a similar length of 20 ± 2 μm.

2.2. Core−Shell Nanowire-Based Photoanodes. Three types of photoanodes were prepared: (1) nanowires (control); (2) nanowires coated with HfO_2 compact layer via ALD; and (3) nanowires coated with TiO_2 compact layer via ALD. A Cambridge Nano Fiji 200 ALD system was used and the precursors for Hf and Ti were tetrakis-(dimethylamido)hafnium(IV) and tetrakis(dimethylamido)titanium-(IV), respectively. Water was used as the O source in both reactions. All ALD depositions were performed in "exposure mode", in which long reaction times were used to ensure uniform axial coating. All nanowires were subsequently coated with a porous TiO_2 shell of different thickness by $TiCl_4$ treatment. A 4.7 M $TiCl_4$ stock solution was prepared using $TiCl_4$ (near 0 °C) and ice. The stock solution was diluted to 0.1 M, and nanowires were immersed in the coating solution for 8 h at room temperature. The coating process could be repeated multiple times to control the thickness of the coating.

2.3. Fabricating DSSC Cells. The nanowire-based photoanodes were annealed at 500 °C for 1 h in air. N719 dye (Dyesol, Australia) was dissolved in ethanol (3 mM concentration) and dye uptake was performed at room temperature for ∼12 h. Counter electrodes were prepared by spin-coating a Pt counter electrode solution (CELS, Dyesol) on clean ITO/glass and annealing at 430 °C for 10 min. DSSC cells were assembled by combining the nanowire-based photoanode and counter electrode with clips. Scotch tape was used as the spacer and an I^-/I_3^--based solution (EL-HPE, Dyesol) was used as the electrolyte. Electrical contact was established from ITO using alligator clips. We determined the amount of dye loading on nanowires by immersing nanowires in a 0.1 M NaOH water/ethanol (1:1 v/v) solution and measuring the absorption spectrum using a PerkinElmer Lambda 800 UV−vis spectrometer (see typical spectra in the Supporting Information).

2.4. Characterization. The morphology of as-grown nanowires was inspected by a field-emission scanning electron microscope (FEI Nova NanoSEM 430). X-ray diffraction (XRD) patterns were recorded by an X'Pert Powder XRD (PANalytical, Westborough, MA). TEM imaging was performed on a JEOL 2010F. A global AM 1.5 spectrum with a power density of 100 mW·cm^{-2} was produced by a simulated light source (XPS 200 coupled with 16S, Solar Light Company, Glenside, PA). A Si reference cell (RCSi65, PV Measurements, Boulder, CO) was used to calibrate the light source before device testing. A potentiostat (VersaSTAT 3, Princeton Applied Research, Oak Ridge, TN) was used to collect $J-V$ curves and perform open-circuit voltage decay (OCVD) measurements. Multiple devices were tested for each type of cell. A two-terminal setup was established by combining working/sensing electrodes and reference/counter electrodes. During OCVD measurements, cells were illuminated to reach a constant open-circuit voltage (V_{oc}) and illumination was interrupted. The transient V_{oc} during the relaxation from the illuminated quasi-equilibrium state to the dark equilibrium was recorded. Electron lifetime (τ_n) was calculated from the OCVD curve using the expression $\tau_n = (-k_BT/e)(dV_{oc}/dt)^{-1}$, where k_B is the Boltzmann constant, T is the absolute temperature, and e is the positive electron charge.

3. RESULTS AND DISCUSSION

3.1. Photoanode Structure. Figure 1a shows a SEM image of the vertically-aligned ITO nanowires. Their direct contact with the ITO substrate is expected to facilitate efficient electron transport during DSSC operation. Because the length of the nanowires has been shown to impact the photovoltaic properties of DSSCs,[10,14] only ITO nanowires of the same length (20 ± 2 μm) were used in this study. Figure 1b shows the XRD pattern of the ITO nanowires. The peak with the highest intensity is (400) instead of (222), indicating that (400) is the predominant growth direction for ITO nanowires. The HRTEM image in Figure 1c shows a single nanowire with a d-spacing of 0.485 nm along the nanowire growth direction, corresponding to the interplanar distance of (400) that was also observed in the XRD spectra. The d-spacing of 0.485 nm is smaller than the d-spacing of pure In_2O_3 (0.505 nm[20]), which indicates successful doping of SnO_2 into In_2O_3. Figure 1d shows a TEM image of the ITO-TiO_2 core−shell nanowires. The TiO_2 coating covered the nanowire surface uniformly and high-magnification TEM images revealed that the coating is porous in nature (Figure S1, Supporting Information), providing a large surface area for dye attachment.

3.2. Effect of HfO_2 Blocking Layer Thickness on Cell Performance. To reduce electron recombination from the ITO nanowire surfaces to the I_3^- in the electrolyte, we deposited HfO_2 blocking layers ranging between 6 and 20 ALD cycles on the as-grown ITO nanowires. The nanowires were then coated with a porous TiO_2 shell by $TiCl_4$ treatment. The thickness of all TiO_2 shells was ∼60 nm after annealing. DSSC devices were assembled using these core−shell nanowires as the photoanode. Figure 2a shows the corresponding $J-V$ curves

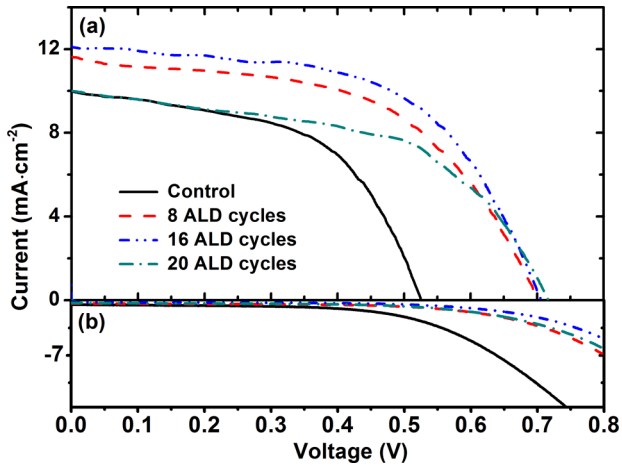

Figure 2. $J-V$ characteristics of nanowire-based cells with different ALD cycles of HfO_2 inserted as blocking layers between the ITO nanowires and porous TiO_2 shell under (a) AM 1.5 illumination and (b) dark conditions.

under AM 1.5 illumination and Table 1 summarizes the photovoltaic properties of these cells. The amount of dye loading for different cells is also included in Table 1. It is seen that HfO_2 insertion between the ITO and TiO_2 interface slightly increases the dye loading of the cells, as also observed by Ramasamy et al.[21] for nanoparticle-based systems. However, the performance enhancement observed here is substantially higher than the increase in dye loading, suggesting that other factors are responsible for the increase in efficiency. Without any HfO_2, the control cell has an efficiency of 2.82%. The relatively low efficiency of the control cell is due to the significantly lower open-circuit voltage (V_{oc}); typically, nanoparticle-based DSSCs have V_{oc} ∼0.7 V. The V_{oc} does increase monotonically with an increase of ALD cycles and eventually

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Table 1. Photovoltaic Properties of Nanowire-Based Cells with Different ALD Cycles of HfO_2 Inserted as Blocking Layers between the ITO Nanowires and Porous TiO_2 Shell[a]

	V_{oc} (V)	J_{sc} (mA·cm^{-2})	FF (%)	η (%)	dye loading ($\times 10^{-8}$ mol·cm^{-2})
control	0.52 ± 0.03	9.96 ± 0.07	54.2 ± 0.9	2.82 ± 0.08	1.51
8 ALD cycles	0.70 ± 0.02	11.62 ± 0.06	53.7 ± 0.7	4.36 ± 0.08	1.58
16 ALD cycles	0.71 ± 0.03	12.17 ± 0.06	55.8 ± 0.6	4.83 ± 0.09	1.61
20 ALD cycles	0.72 ± 0.04	10.01 ± 0.08	53.3 ± 1.0	3.83 ± 0.06	1.62

[a]Average values and standard deviations are based on 3−4 devices.

reaches 0.717 V after 20 ALD cycles, corresponding to an enhancement of 37% from the control. The increase of V_{oc} due to the insertion of blocking layers on TCO has also been reported for nanoparticle-based DSSCs.[22] The increase of V_{oc} is attributed to the negative shift of the conduction band (CB) edge of TiO_2 upon inserting the blocking-layer between ITO and TiO_2 since the CB edge position of the blocking layer is more negative than TiO_2. However, the dramatic difference in V_{oc} shown in Figure 2a suggests that electron recombination was significantly altered as well. When electron recombination is significant, the V_{oc} of the cell is reduced. Indeed, Figure 2b shows the dark current decreased with an increase of ALD cycles. Because dark current flows in the reverse direction of illuminated cells, the smaller dark current observed with HfO_2 layers indicates a lower rate of electron recombination.

In contrast to the steady increase in V_{oc}, the short-circuit current (J_{sc}) increased initially with the number of ALD cycles but then decreased at 20 ALD cycles. The increase in J_{sc} results from the energy barrier established by HfO_2 between ITO and TiO_2 that reduced electron recombination and raises the Fermi level. A thin HfO_2 layer allows electrons to tunnel through from TiO_2 to ITO while suppressing their backflow. However, the tunneling probability of electrons falls as they transport through thicker HfO_2 layers. Consequently, a lower J_{sc} is observed in Figure 2a for barrier layers greater than 16 ALD cycles (~1.3 nm, as described further below). The improvement of both V_{oc} and J_{sc} leads to the highest efficiency of 4.83% at 16 ALD cycles, corresponding to an efficiency enhancement of 71% from the control cell.

Further confirmation of electron recombination improvement is observed in the OCVD measurements of cells with different ALD cycles of HfO_2 between the ITO nanowires and porous TiO_2 shell, as shown in Figure 3a. The V_{oc} showed slower decay as the number of ALD cycles increased to 16 cycles, indicating progressively reduced electron recombination for thicker blocking layers. The V_{oc} showed faster decay at 20 cycles, which corresponds well to the decreased cell efficiency from 16 to 20 cycles (Table 1). The calculated electron lifetime shown in Figure 3b is seen to increase with the increased ALD cycles to 16 cycles. Figure 3c shows the electron lifetime as a function of the number of ALD cycles at a constant voltage of V = 0.4 V. Compared to the control cell, the electron lifetime increased by more than 1 order of magnitude with 16 cycles of HfO_2 on ITO nanowires (from 0.028 to 0.36 s). The increased electron lifetime results in the highest J_{sc} and efficiency, as seen in Figure 2a and Table 1.

3.3. Effect of Porous TiO_2 Coating Thickness on Cell Performance. Because 16 ALD cycles of HfO_2 deposited on ITO nanowires yielded the best efficiency, these structures were used to investigate the thickness of the porous TiO_2 on the photoanode. These structures were coated with 45, 70, and 90 nm of porous TiO_2 (see Figure S1, Supporting Information, for TEM images of the porous TiO_2 of different thickness).

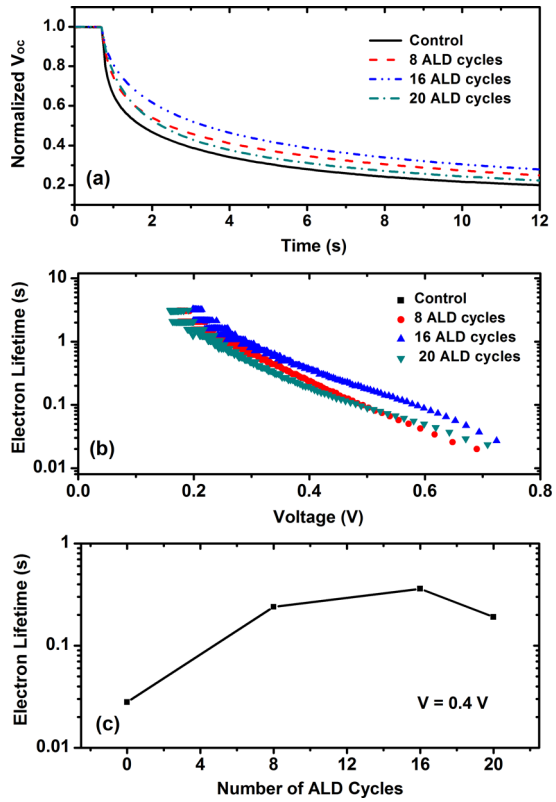

Figure 3. (a) OCVD curves and (b) electron lifetimes of nanowire-based cells with different ALD cycles of HfO_2 inserted as blocking layers between the ITO nanowires and porous TiO_2 shell. (c) Electron lifetimes at different numbers of ALD cycles at 0.4 V (the line is drawn for visual aid).

Devices were made, and their $J-V$ characteristics are shown in Figure 4 and summarized in Table 2. Thicker TiO_2 shells led to a reduction in V_{oc}, which is due to the positive shift of the CB edge of the semiconductor upon more TiO_2 addition. In contrast, J_{sc} was a maximum when the TiO_2 thickness was 70 nm. The initial increase in J_{sc} is due to the higher dye loading associated with a thicker TiO_2 shell (Table 2). Above a TiO_2 thickness of 70 nm, dye loading continued to increase; however, slower charge transport through the TiO_2 shell leads to more severe electron recombination, as characterized by the higher dark current in Figure 4b. The electron loss due to electron recombination exceeded the electron gain due to higher dye loading, resulting in an overall reduction in J_{sc} with 90 nm of TiO_2.

3.4. Effect of Energy Barrier Height on Cell Performance. Both HfO_2 and TiO_2 blocking layers were deposited on the as-grown ITO nanowires with identical thicknesses. Figure 5 shows TEM images of the as-grown nanowires and nanowires coated with either HfO_2 or TiO_2. Both coatings had a thickness

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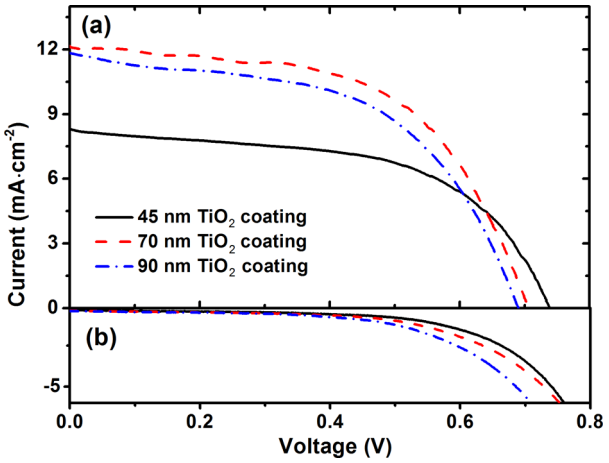

Figure 4. $J-V$ curves of nanowire-based cells with different thicknesses of a porous TiO_2 shell over a HfO_2 layer (16 ALD cycles) on ITO nanowires under (a) AM 1.5 illumination and (b) dark conditions.

of 1.3 nm, which should be thin enough to allow efficient tunneling.[23] Subsequently, a porous TiO_2 shell with a thickness of 70 nm was simultaneously coated on both types of ITO nanowires by $TiCl_4$ treatment. DSSC devices were fabricated using these nanowires as the photoanode and their photovoltaic properties were evaluated.

Figure 6 shows the $J-V$ curves of cells with different blocking layer composition compared to the control cell without ALD deposition. Photovoltaic properties of the cells are summarized in Table 3. With the addition of a compact layer of either TiO_2 or HfO_2, both V_{oc} and J_{sc} increased from the control cell, leading to much higher device efficiencies. Figure 6b shows that the corresponding dark current for both HfO_2 and TiO_2 compact blocking layers was lower than the control cell. The dark current for HfO_2 is lower than TiO_2, indicating a lower rate of electron recombination in the cell with a HfO_2 compact layer. For this reason, the HfO_2-based cell has a better fill factor and a V_{oc} ~70 mV higher than that of TiO_2. Surprisingly, the efficiency of the cell with the HfO_2 blocking layer did not exceed the cell with the TiO_2 layer. The cells based on TiO_2 compact blocking layers showed a higher efficiency of 5.38% due to the substantial increase in J_{sc}.

Compared to the substantial efficiency increase in nanowire-based DSSCs (from 2.82 to 5.38%, a 91% increase), the efficiency increase in nanoparticle-based DSSCs using blocking layers is generally moderate. For example, we recently studied the effect of HfO_2 blocking layers on different interfaces of nanoparticle-based DSSCs, and the efficiency only increased by ~10%.[16] A comparison of the performance between the two architectures is shown in Figure 7. The nanowire-based DSSCs without HfO_2 blocking layers have much higher dark current in Figure 7a than in their nanoparticle counterparts, which suggests that nanowire DSSCs suffer much more severe

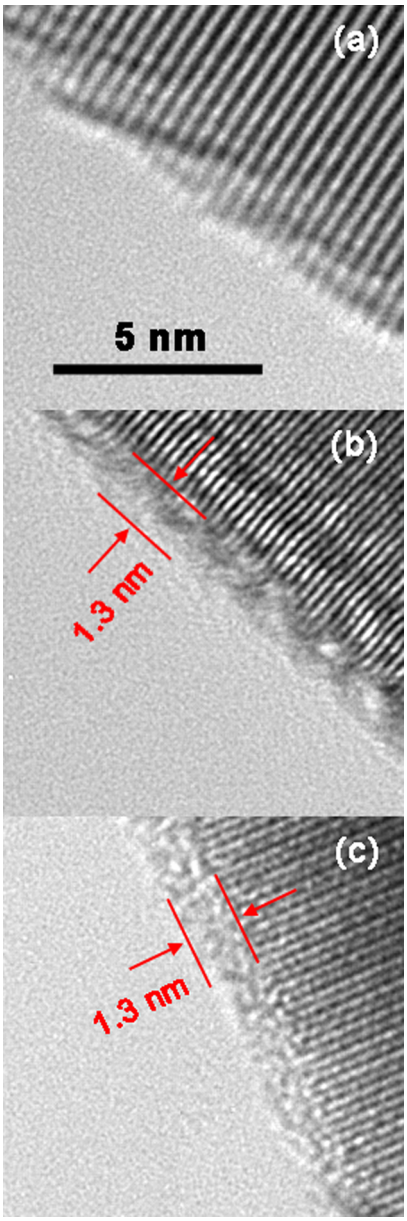

Figure 5. TEM images of ITO nanowires (a) without blocking layer, (b) with a 1.3 nm thick HfO_2 blocking layer, and (c) with a 1.3 nm thick TiO_2 blocking layer.

electron recombination. The higher recombination could be caused by the increased interaction of ITO with the electrolyte, a relatively higher level of defects at the surface of the ITO nanowires, or the effect of the morphology on specific reactions.[7] After inserting the HfO_2 blocking layers, the dark current shows a greater reduction in nanowire-based DSSCs. Interestingly, the nanowire-based devices now show better dark

Table 2. Photovoltaic Properties of Nanowire-Based Cells with Different Thicknesses of a Porous TiO_2 Shell over a HfO_2 Layer (16 ALD cycles) on ITO Nanowires[a]

	V_{oc} (V)	J_{sc} (mA·cm^{-2})	FF (%)	η (%)	dye loading (×10^{-8} mol·cm^{-2})
45 nm TiO_2	0.74 ± 0.05	8.30 ± 0.03	55.8 ± 0.4	3.42 ± 0.06	1.25
70 nm TiO_2	0.71 ± 0.03	12.17 ± 0.06	55.8 ± 0.6	4.83 ± 0.09	1.61
90 nm TiO_2	0.69 ± 0.02	11.82 ± 0.07	53.5 ± 0.9	4.37 ± 0.07	1.89

[a]Average values and standard deviations are based on 3–4 devices.

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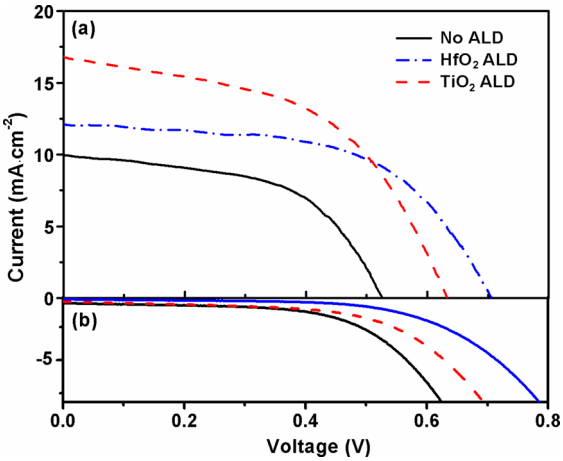

Figure 6. $J-V$ curves of nanowire-based cells with either HfO_2 or TiO_2 compact blocking layers deposited via ALD under (a) AM 1.5 illumination and (b) dark conditions. All nanowires have the same thickness of the compact blocking layer (1.3 nm) and are identically coated with a 70 nm thick porous TiO_2 shell.

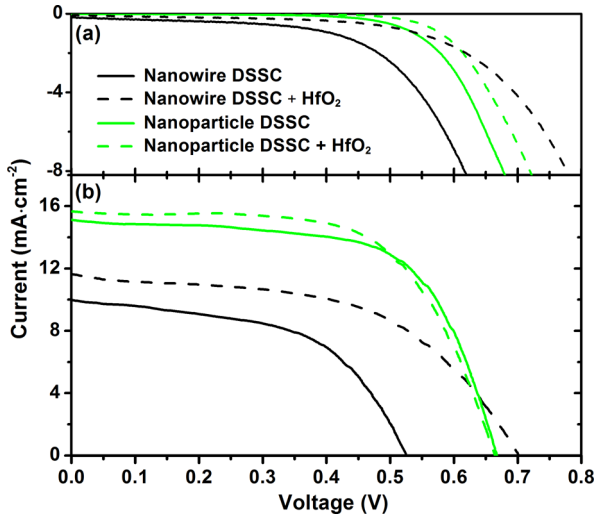

Figure 7. Comparison of $J-V$ curves between nanowire- and nanoparticle-based DSSCs (a) in the dark and (b) under AM 1.5 illumination. The nanoparticle devices were originally reported in our previous work,[16] which consisted of a 12 μm thick TiO_2-nanoparticle–film on a flat ITO substrate as the photoanode. For HfO_2 deposition, 8 and 6 ALD cycles were performed on the ITO nanowires (this work) and the flat ITO substrate, respectively.

current responses than the nanoparticle-based devices. This result is in agreement with previous studies that alleged that nanowires should have lower recombination than nanoparticle systems because of the electric field established at the interface.[4,7] However, this work demonstrates that this effect only becomes evident once the interface has been passivated.

Although the dark current is better in the nanowire-based DSSCs, their efficiency is still lower than their nanoparticle counterparts. Figure 7b shows that the short-circuit current is significantly lower in the nanowire-based devices. This difference is attributed to the lower surface area and, hence, lower dye-loading, in the nanowire-based devices.[3,9] The surface area of the nanowire-based DSSCs is conservatively an order of magnitude or more lower. Therefore, further efficiency increases are possible if nanowire arrays with much higher packing density can be fabricated. These devices could achieve photoactive (not actual) surface areas comparable to nanoparticle-based DSSCs while maintaining the reduced electron recombination observed here.

To further investigate the kinetics of electron transport in the nanowire DSSCs, we measured the OCVD and electrochemical impedance spectroscopy (EIS). Figure 8a shows OCVD curves for cells with HfO_2 and TiO_2 compact blocking layers. The V_{oc} of HfO_2–based devices decayed slower than TiO_2–based devices, suggesting a lower rate of recombination for HfO_2 compact blocking layers in agreement with the $J-V$ measurements. During OCVD measurements, electron loss can occur by recombination from TiO_2 to either the I_3^- or oxidized dye (although recombination with I_3^- is believed to be dominant). Electron loss can also occur from the ITO nanowires.[5] Because

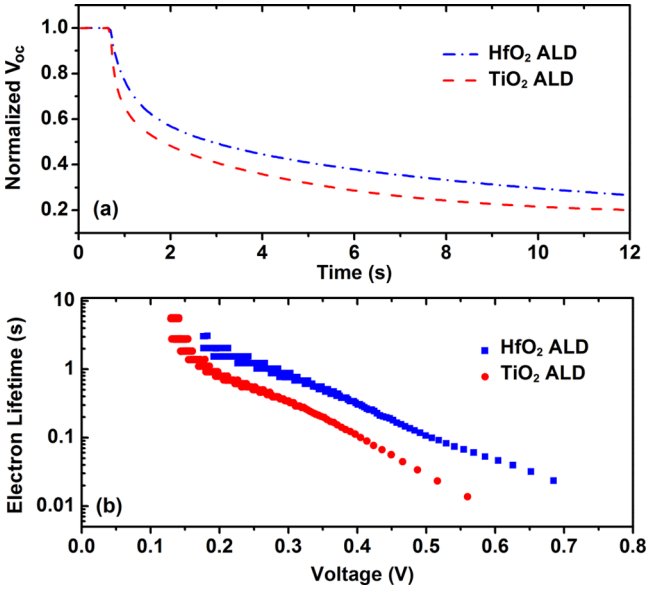

Figure 8. (a) OCVD curves and (b) electron lifetime of nanowire-based cells with either HfO_2 or TiO_2 compact blocking layers deposited via ALD. All nanowires have the same thickness of the compact blocking layer (1.3 nm) and are identically coated with a 70 nm thick porous TiO_2 shell.

Table 3. Photovoltaic Properties of Nanowire-Based Cells with Either HfO_2 or TiO_2 Compact Blocking Layers Deposited via ALD[a]

	V_{oc} (V)	J_{sc} (mA·cm^{-2})	FF (%)	η (%)	dye loading (×10^{-8} mol·cm^{-2})
control	0.52 ± 0.03	9.96 ± 0.07	54.2 ± 0.9	2.82 ± 0.08	1.51
HfO_2 ALD	0.71 ± 0.03	12.17 ± 0.06	55.8 ± 0.6	4.83 ± 0.09	1.61
TiO_2 ALD	0.63 ± 0.04	16.80 ± 0.05	50.7 ± 0.7	5.38 ± 0.05	1.57

[a]Average values and standard deviations are based on 3–4 devices. All nanowires have the same thickness of the compact blocking layer (1.3 nm) and are identically coated with a 70 nm thick porous TiO_2 shell.

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all dimensions were the same, the only variation between the two types of cells is the blocking layer composition. Therefore, the observed difference in OCVD curves is attributed to different recombination rates from ITO nanowires to I_3^-. The lower recombination rate for HfO_2 compact blocking layers is due to the energy barrier established by HfO_2 between the ITO nanowires and the porous TiO_2 shell. Consequently, the HfO_2–based devices have a higher electron lifetime than TiO_2–based devices (Figure 8b), which was also observed in EIS measurements (Supporting Information).

To elucidate the electron transfer processes in different photoanodes, we show a schematic band diagram during charge transport in DSSCs (Figure 9). The control cell consists of a

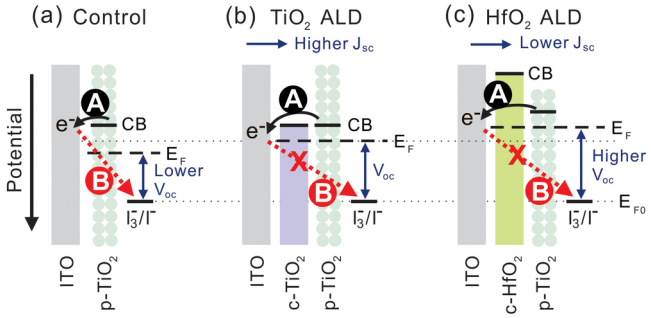

Figure 9. Schematic of electron transport processes in different photoanode structures. (a) Control cell where ITO nanowires are coated with a porous TiO_2 shell (p-TiO_2); (b) a compact TiO_2 layer (c-TiO_2) inserted between ITO nanowires and porous TiO_2; and (c) a compact HfO_2 layer (c-HfO_2) inserted between ITO nanowires and porous TiO_2. In the diagram, A represents charge transport from TiO_2 to ITO, B represents electron recombination from ITO to I_3^- electrolyte, E_F is the Fermi level of the semiconductor, and E_{F0} is the Fermi level of the redox couple. Note the energy levels for the dye are omitted for simplicity.

porous TiO_2 shell deposited on ITO nanowires. As shown in Figure 9a, the porous TiO_2 shell allows direct contact between ITO nanowires and the electrolyte. Upon electron transport from TiO_2 to ITO nanowires (process A), electron recombination occurs readily from ITO to I_3^- in the electrolyte (process B).[5] The V_{oc} of DSSCs is determined by the Fermi level of the semiconductor and that of the redox couple in the electrolyte. Therefore, the electron loss associated with process B will reduce the Fermi level of TiO_2 and consequently reduce V_{oc}.[24] The low V_{oc} of 0.52 V seen in Figure 6 for the control suggests a significant loss of electrons.

Although nanoparticle-based DSSCs typically have a similar porous layer on an ITO substrate, the nanowire array increases the surface area of the current collector. Therefore, electron recombination losses from ITO (nanowires and substrate) may be more significant than nanoparticle-based devices, explaining why the control devices have much lower V_{oc} and require thicker blocking layers to be effective.

When a compact TiO_2 layer is inserted (e.g., via ALD) between the ITO nanowires and the porous TiO_2, direct contact between ITO and the electrolyte is eliminated and the electron recombination associated with process B is greatly reduced, as shown in Figure 9b. This reduction can be seen by the smaller dark current upon TiO_2 insertion in Figure 6b. The increased Fermi level in the TiO_2 layer raises V_{oc}, as seen in Figure 6a, while the reduced electron recombination results in higher J_{sc}. The insertion of a thin (1.3 nm), compact TiO_2 layer ultimately led to an efficiency enhancement of more than 90% (Table 3). Sol–gel methods (e.g., $TiCl_4$ treatment) have been commonly used to deposit TiO_2 in DSSCs[18] because of their low cost and practicality. However, the above observation implies that coatings deposited by sol–gel methods are inadequate as blocking layers for nanowire-based devices because of the porous nature of these coatings and the greater importance of electron loss from the current collector. Instead, compact coatings formed by ALD are more advantageous as blocking layers.

When the compact layer composition is changed to HfO_2, the highest V_{oc} is observed (Figure 9c and Table 3). The increased V_{oc} is partly attributed to a rise in the Fermi level of the semiconductor due to the reduced recombination from ITO to the electrolyte. The more negative CB edge position of HfO_2 compared to TiO_2 could also contribute to the higher V_{oc} observed.[25] Interestingly, HfO_2 insertion showed lower J_{sc} than TiO_2 for the same thickness (Table 3). The lower J_{sc} for HfO_2 insertion resulted from the more negative CB edge position of HfO_2 that forms an energy barrier and suppresses charge transfer associated with process A in Figure 9c.

While the TiO_2 and HfO_2 blocking layers both work similarly, there is a key difference. TiO_2 reduced process B without impacting process A. HfO_2 does a better job of reducing process B but suppresses process A. Ultimately, the balance led to a higher efficiency for TiO_2–based devices. Although thin blocking layers with a high CB edge position are widely exploited to reduce electron recombination in nanoparticle-based DSSCs,[15,16] the lower J_{sc} for HfO_2 blocking layers suggests that the suppression of charge collection by blocking layers may limit their effectiveness in nanowire-based DSSCs. Therefore, the insertion of high band gap materials between the conductive nanowire and the porous TiO_2 shell is not recommended due to the more severe ITO-electrolyte electron recombination in these systems.

4. CONCLUSIONS

Photoanodes based on ITO nanowires with a porous TiO_2 shell of different thicknesses were fabricated to investigate the role of blocking layers. Because of the greater importance of electron recombination losses from ITO to I_3^- in nanowire-based DSSCs, a thin compact blocking layer is necessary to enhance device performance. A compact layer of either TiO_2 or HfO_2 was inserted between the nanowires and the porous TiO_2 shell by ALD. The use of 16 ALD cycles of HfO_2 increased device efficiencies from 2.82 (no HfO_2) to 4.83%. A thicker TiO_2 shell increased dye loading and, consequently, the short-circuit current; however, more severe electron recombination occurred as well. Optimal performance is obtained by balancing dye loading and electron recombination. The insertion of a TiO_2 compact blocking layer between the ITO nanowires and the porous TiO_2 shell led to a device efficiency of 5.38%, which is more efficient than a HfO_2 blocking layer of identical thickness. Investigation of the charge transport reveals that suppression of charge collection by blocking layers plays an important role in the performance of nanowire-based devices. Therefore, the use of high band gap materials inserted between the conductive nanowire and the porous TiO_2 shell is not recommended.

■ ASSOCIATED CONTENT

Supporting Information

TEM images of TiO_2-coated nanowires, UV–vis spectra for measuring dye loading, and Bode phase plot from EIS

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AUTHOR INFORMATION

Corresponding Authors

*E-mail: kziegler@che.ufl.edu.
*E-mail: lupingli@ufl.edu.

Notes

The authors declare no competing financial interest.

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